

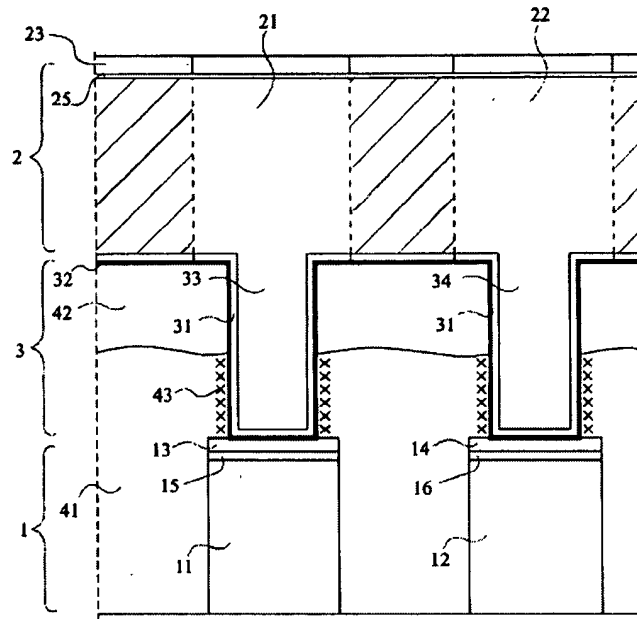
Remarks

Claims 1, 2 and 4–7 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,180,520 ("Marty"). Claims 1–7 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 5,877,080 ("Aoi"). Claims 8 and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Marty in view of U.S. Patent 5,869,379 ("Gardener") or Aoi in view of Gardener.

Claim Rejections Under § 102(e) based on Marty.

Claims 1, 2 and 4–7 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,180,520 ("Marty"). Claims 1 and 5 are independent; Claims 2 and 4 depend from Claim 1, and Claims 6 and 7 depend from Claim 5.

Marty discloses an interconnect structure having a first metallization level 1 and a second metallization level 2, that are connected by vias 11–33 and 12–34. Two distinct insulating layers 41 and 42 are disposed between the metallization levels. Specifically, a first insulating layer 41 having a relatively low dielectric constant contacts the first metallization level 1, while a second insulating layer 42 having a relatively high dielectric constant contacts the second metallization level 2. This structure is illustrated in Figure 1 of Marty, which is reproduced below.



In contrast to the structure disclosed in Marty, Applicant has amended Claim 1 to recite:

Claim 1: An interconnect structure comprising:

a first planar network of electrical conductors formed in a first deposition process;

a second planar network of electrical conductors formed in a second deposition process, and separated from the first planar network by a separation region; and

a single interlevel dielectric material disposed within the separation region and extending into a portion of the first planar network, without other intervening insulating materials between the first and second planar networks, **such that the interlevel dielectric material has a planarized surface that interfaces the second planar network of electrical conductors**, the interlevel dielectric material comprising a polysiloxane network consisting essentially of silicon, oxygen, carbon and hydrogen and incorporating carbon-silicon bonding and having a dielectric constant of less than about 3.3. *[emphasis added]*

Marty does not teach these limitations. Marty teaches that the insulating agent used between and over portions (11, 12) is an organic spun on glass ("SOG") material made of a polysiloxane material that includes an alcohol as a diluting agent (3:25–31). Marty designates the SOG layer with reference numeral 41 (3:57–58). However, Marty notes that the upper surface of the SOG layer "is actually not perfectly planar at the submicrometric scale," and therefore that it is preferred to deposit back over the SOG

layer a TEOS layer, indicated by reference numeral 42 (3:58–62). After depositing the TEOS layer, Marty teaches that it is then possible to proceed to a chemical and mechanical planarization step (3:62–64).

The Examiner has taken the position that Marty teaches a “non-preferred embodiment” that excludes the TEOS layer. Initially, expressing a “preference” for the second insulator does not make the absence of that insulator an “embodiment,” non-preferred or otherwise. Such a position would enable the Examiner to omit practically any element from patent teachings without any suggestion for modification. Patent disclosures have a tendency to describe all features as “preferences” to broaden their claim scope. To depart from a reference’s positive teachings, whether preferences or otherwise, the Examiner must show the **desirability** of the modification from the prior art. The absence of a preferred feature is **neither** a positively taught embodiment **nor** a suggestion.

Furthermore, nowhere has the Examiner shown the desirability of a non-planar insulator by omission of Marty’s preferred second insulator. From a practical standpoint, the TEOS layer is necessary in Marty’s process, particularly if a planarized surface is to be obtained on the insulating layer. Marty does not teach how to obtain a planarized surface without use of a second insulating layer deposited over the SOG layer.

Amended Claim 1 recites, among other elements, that “the interlevel dielectric material has a planarized surface that interfaces the second planar network of electrical conductors”. Marty does not teach this element. In Marty’s preferred embodiment, there are multiple interlevel dielectric materials. Even accepting the Examiner’s unmotivated modification, Marty’s “non-preferred embodiment,” wherein the TEOS layer is not deposited back over the SOG layer, the SOG layer, by Marty’s own teaching, would be “not perfectly planar at the submicrometric scale,” and therefore would not be a “planarized surface”.

In view of the foregoing, Applicant submits that Marty does not anticipate Claim 1, and therefore respectfully suggests that Claim 1 is allowable over Marty. Furthermore, because Claims 2 and 4 depend from Claim 1, Applicant submits that

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Claims 2 and 4 are allowable over Marty for the same reasons that Claim 1 is allowable over Marty, in addition to reciting further distinguishing features of particular utility.

Likewise, Applicant has amended Claim 5 to recite:

Claim 5: An integrated circuit comprising:

a first planar network of electrical conductors formed in a first deposition process, and providing a first electrical path of the circuit;

a second planar network of electrical conductors formed in a second deposition process, and providing a second electrical path of the circuit, the second planar network separated from the first planar network by a gap; and

an interlevel dielectric material directly contacting the first and second planar networks, filling the gap between the first and second planar networks, **having a planarized surface interfacing with the second planar network**, and extending into a portion of the first planar network, the interlevel dielectric material comprising polysiloxane, consisting essentially of silicon, oxygen, carbon and hydrogen and incorporating carbon therein and having a dielectric constant of less than about 3.5. *[emphasis added]*

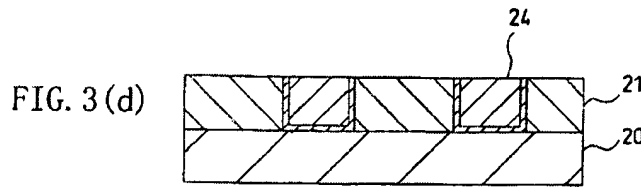
Marty does not teach these elements. As described above, in Marty's preferred embodiment, there are multiple interlevel dielectric materials. In Marty's "non-preferred embodiment," wherein the TEOS layer is not deposited back over the SOG layer, the SOG layer is, by Marty's own teaching, "not perfectly planar at the submicrometric scale," and therefore is not a "planarized surface".

In view of the foregoing, Applicant submits that Marty does not anticipate Claim 5, and therefore respectfully suggests that Claim 5 is allowable over Marty. Furthermore, because Claims 6 and 7 depend from Claim 5, Applicant submits that Claims 6 and 7 are allowable over Marty for the same reasons that Claim 5 is allowable over Marty, in addition to reciting further distinguishing features of particular utility.

Claim Rejections Under § 102(e) based on Aoi.

Claims 1–7 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 5,877,080 ("Aoi"). Claims 1 and 5 are independent; Claims 2–4 depend from Claim 1, and Claims 6 and 7 depend from Claim 5.

As characterized by the Examiner, Aoi discloses first and second conductive elements 24 (horizontally) separated from each other by a gap, with a single insulating layer 21 directly contacting the first and second conductive elements 24. This structure is illustrated in Figure 3(d) of Aoi, which is reproduced below.



In contrast to the structure disclosed in Aoi, amended Claim 1 recites:

Claim 1: An interconnect structure comprising:

a first planar network of electrical conductors formed in a first deposition process;

a second planar network of electrical conductors formed in a second deposition process, and separated from the first planar network by a separation region; and

a single interlevel dielectric material disposed within the separation region and extending into a portion of the first planar network, without other intervening insulating materials between the first and second planar networks, such that the interlevel dielectric material has a planarized surface that interfaces the second planar network of electrical conductors, the interlevel dielectric material comprising a polysiloxane network consisting essentially of silicon, oxygen, carbon and hydrogen and incorporating carbon-silicon bonding and having a dielectric constant of less than about 3.3.

Aoi does not teach this limitation. For example, in the Aoi structure described and illustrated above, there are intervening materials between the first and second conductive elements 24. Additionally, the Aoi structure's insulating layer 21 is not an interlevel dielectric, since the single insulating layer 21 does not contact successive metallization levels, but rather contacts conductors on the same level of the integrated circuit.

In the Office Action mailed on 9 September 2003, the Examiner has taken the position that Aoi "teaches that an upper metallization layer is formed on the insulating film," citing Claim 1 of Aoi. However, "the scope of a patent's claims determines what infringes the patent; it is no measure of what it discloses." *In re Benno*, 768 F.2d 1340, 1346 (Fed. Cir. 1985). Therefore, it is irrelevant whether the claims of Aoi are broad enough to read on the structure recited in Claim 1 of the present application. In particular, Aoi's Claim 1 does not disclose anything more than what Aoi's specification discloses.

Applicant thus submits that Aoi does not anticipate Claim 1, and therefore respectfully submits that Claim 1 is allowable over Aoi. Furthermore, because Claims

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2–4 depend from Claim 1, Applicant submits that Claims 2–4 are allowable over Aoi for the same reasons that Claim 1 is allowable over Aoi, in addition to reciting further distinguishing features of particular utility.

Likewise, in contrast to the structure disclosed in Aoi, amended Claim 5 recites:

Claim 5 : An integrated circuit comprising:
a first planar network of electrical conductors formed in a first deposition process, and providing a first electrical path of the circuit;
a second planar network of electrical conductors formed in a second deposition process, and providing a second electrical path of the circuit, the second planar network separated from the first planar network by a gap; and
an interlevel dielectric material directly contacting the first and second planar networks, filling the gap between the first and second planar networks, having a planarized surface interfacing with the second planar network, and extending into a portion of the first planar network, the interlevel dielectric material comprising polysiloxane, consisting essentially of silicon, oxygen, carbon and hydrogen and incorporating carbon therein and having a dielectric constant of less than about 3.5.

Again, Aoi does not teach this limitation. As described above, the Aoi structure's insulating layer 21 is not an interlevel dielectric, since the single insulating layer 21 does not contact successive metallization levels, but rather contacts conductors on the same level of the integrated circuit. It is irrelevant whether Aoi's claims are broad enough to read on the structure recited in Claim 5 of the present application.

Applicant thus submits that Aoi does not anticipate Claim 5, and therefore respectfully submits that Claim 5 is in condition for allowance. Furthermore, because Claims 6 and 7 depend from Claim 5, Applicant submits that Claims 6 and 7 are allowable over Aoi for the same reasons that Claim 5 is allowable over Aoi, in addition to reciting further distinguishing features of particular utility.

Claim Rejections Under § 103(a).

Claims 8 and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Marty in view of U.S. Patent 5,869,379 ("Gardener") or Aoi in view of Gardener. Claims 8 and 9 depend from Claim 5. Gardner does not provide the deficiencies of Marty or Aoi. Because Claims 8 and 9 depend from Claim 5, Applicant respectfully submits that Claims 8 and 9 are allowable for the same reasons explained above, in addition to reciting further distinguishing features of particular utility.

Conclusion.

In view of the foregoing amendments, the Applicants submit that this application is in condition for allowance, and respectfully request the same. If, however, some issue remains that the Examiner feels can be addressed by an Examiner's Amendment, the Examiner is cordially invited to call the undersigned for authorization.

Respectfully submitted,

KNOBBE MARTENS OLSON & BEAR LLP

Dated: 9 July 2004

By: Kyle F. Schlueter
Kyle F. Schlueter
Registration No. 54,912
Attorney of Record
Customer No. 20,995
(310) 551-3450